Lakshya Varshney

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LinkedIn GitHub Portfolio Credly

Education

COEP Technological University **Pune, Maharashtra**

B.Tech. in Electronics and Telecommunication Engineering (CGPA: 8.16/10) *Expected July 2029*

- **Relevant Coursework:** Formal Hardware Verification, Embedded Systems, VLSI Design, Compilers & Systems, Data Structures.

Experience & Technical Leadership

Systems Developer & Communications Contributor **Nov 2025 – Present**

COEP Satellite Initiative (CSAT-2) *Pune, Maharashtra*

- Engineered **NEST**, an enterprise system of record migrating asset and telemetry tracking from spreadsheets to a searchable, auditable, role-gated platform using React, NestJS, and PostgreSQL.

Technical Event Head — Circuit Fixer **Oct 2026**

MindSpark '26, COEP Technological University *Pune, Maharashtra*

- Spearheaded problem design and bench evaluation for COEP's flagship hardware debugging competition, diagnosing op-amp stability, digital IC race conditions, and circuit faults for **200+ collegiate participants**.

Systems, EDA & Safety-Critical Projects

LogiSAT: Automated Circuit Equivalence & Fault Verifier (ATPG) | *ISO C99, DPLL, GTest* **Oct 2026**

- Built an open-source formal EDA tool in strict ISO C99 with zero dynamic heap allocation during search trail exploration (GitHub | DOI: 10.5281/zenodo.24085901).
- Engineered recursive linear-size Tseytin 3-CNF transform, Miter circuit synthesis for Combinational Equivalence Checking (CEC), and Automatic Test Pattern Generation (ATPG) for single stuck-at faults (s-a-0 / s-a-1).
- Implemented DPLL solver with Unit Clause Propagation (BCP), DLIS branching heuristic, and automated Google Test regression (**12/12 unit tests passing, Valgrind certified zero leaks**) under `-Wall -Wextra -pedantic`.

MISRA-C Embedded Scientific Calculator | *MISRA C:2012, Static Memory, Embedded C* **Sep 2026 – Oct 2026**

- Developed a safety-critical scientific math evaluation engine strictly adhering to core **MISRA C:2012** guidelines (GitHub | DOI: 10.5281/zenodo.24085926).
- Enforced zero dynamic memory allocation (`malloc` prohibited), fixed-width standard integers (`stdint.h`), bounded static ring buffers, and defensive execution guarantees against undefined behavior.

Aakh: Automated Tech Feed & Model Discovery Pipeline | *Python, GitHub Actions CI/CD, REST API, React* **Aug 2026 – Present**

- Built an automated aggregator leveraging scheduled GitHub Actions workflows to scrape, summarize, and deploy technical feeds (GitHub | Live).
- Implemented dynamic model discovery protocol at runtime querying model provider REST endpoints, preventing failures from LLM deprecation.

Transistor-Level Custom Complementary Logic Modeling | *SPICE, Transistor Primitives, Custom Cell* **May 2026 – July 2026**

- Designed custom logic cell primitives directly at the transistor level using complementary MOSFET networks without HDL abstraction; evaluated propagation delay tradeoffs and switching noise in SPICE.

Technical Skills & Affiliations

Languages & Standards: ISO C99, Lean 4, C++, MISRA C:2012, Python, TypeScript, SQL, Bash, Verilog (Basics)
EDA & Verification Concepts: Formal Equivalence Checking (Miter CEC), SAT Solvers (DPLL Algorithm, DLIS, BCP), Tseytin CNF Conversion, ATPG (Stuck-At Faults), Static Timing Analysis, Combinational Logic Synthesis
Systems Tools & Frameworks: Google Test (GTest), Valgrind, GCC / Clang / MinGW, GNU Make, Lake, Git, PostgreSQL, NestJS, React
Professional Affiliations & Service: Student Member & Volunteer, **IEEE** (IEEE Pune Section; active attendee and student volunteer across conferences and Student Congresses)