Lakshya Varshney

Pune, Maharashtra | +91 7385311907 | creativelakshya.1@gmail.com

LinkedIn GitHub Portfolio Credly

Education

COEP Technological University **Pune, Maharashtra**

B.Tech. in Electronics and Telecommunication Engineering (CGPA: 8.16/10) *Expected July 2029*

- **Focus Areas:** Digital Systems Architecture, Hardware Security, Stochastic Control, Signal Theory, Embedded Systems.

Research & Technical Specifications

Reverse-Logic ASIC Building Block PRD | *Silicon Architecture, Hardware SAT* **Sep 2026**

- Authored Product Requirements Document and circuit architecture for a fabricated 4-variable reconfigurable reverse-logic expression block evaluating physical Boolean constraint propagation.
- Specified reverse AND/OR primitives for PCB constraint networks, targeting hardware-accelerated Boolean satisfiability solving.
- Defined physical pinout constraints, reverse propagation dynamics, and board-level test methodology for silicon fabrication.

LogiSAT: Strict ISO C99 DPLL SAT Solver & Equivalence Checker | *Formal Verification* **Sep 2026 – Oct 2026**

- Developed an automated Boolean satisfiability solver and digital combinational equivalence checker (CEC / ATPG) in strict ISO C99 (DOI: 10.5281/zenodo.24085901 | GitHub).
- Engineered recursive Tseytin 3-CNF conversion, Boolean constraint propagation (BCP), and pure literal elimination with **zero dynamic allocations** (0 heap leaks under Valgrind).
- Empirically benchmarked DPLL branching performance on hard Pigeonhole Principle CNFs and phase transition thresholds ($\alpha \approx 4.26$).

Cognitive Electronic Warfare Spectrum Sensing via POMDP | *DRDO Defense Submission* **Sep 2026 – Oct 2026**

- Formulated dynamic electronic surveillance under receiver bandwidth limits as a 7-tuple Partially Observable Markov Decision Process (**POMDP**) for the Smart India Hackathon DRDO problem statement.
- Derived Bayesian belief-state updates balancing wideband exploration vs. narrowband dwell to classify modulations under negative SNR.

Honors, Leadership & Service

Technical Event Head — Circuit Fixer **Oct 2026**

MindSpark '26, COEP Technological University *Pune, Maharashtra*

- Designed and executed multi-stage hardware troubleshooting competitions evaluating circuit diagnosis for **200+ collegiate participants**.

IEEE Student Member & Conference Volunteer **2025 – Present**

IEEE Pune Section *Pune, Maharashtra*

- Active student volunteer across regional conferences and Student Congresses, assisting with event coordination and technical sessions.

2nd Place — Forbes Marshall Engineering Ideathon **Pune, Maharashtra**

Technical Case Competition *MindSpark / Industry Review*

- Secured 2nd place in engineering design thinking, constraint optimization, and industrial product architecture.

Technical Competencies & Affiliations

Research & Hardware Architecture: Physical Constraint Propagation, Boolean SAT/DPLL Algorithms, POMDP Modeling, Hardware Verification
Programming & Tools: C (Strict ISO C99), Python (NumPy, SciPy), MATLAB, KiCad 8.0, SPICE, Git, Linux, LaTeX
Professional Affiliations & Service: Student Member & Volunteer, **IEEE** (IEEE Pune Section)
Literary Works: Author, *Ink & Infinity*; Featured Poet, COEP Annual Literary Magazine (*The Truth That Walks Alone*)