Lakshya Varshney

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LinkedIn GitHub Portfolio Credly

Education

COEP Technological University **Pune, Maharashtra**

B.Tech. in Electronics and Telecommunication Engineering (CGPA: 8.16/10) *Expected July 2029*

- **Relevant Coursework:** RF & Microwave Engineering, Analog IC Design, VLSI Design, Embedded Systems, Signal Processing.

Experience & Technical Leadership

RF & Communications Subsystem Contributor **Nov 2025 – Present**

COEP Satellite Initiative (CSAT-2) *Pune, Maharashtra*

- Designed and routed a compact 4-layer RF transceiver and switching board in KiCad conforming to CubeSat 1U structural rail cutouts.
- Performed laboratory VNA measurements, impedance matching, and link budget evaluations for VHF/UHF satellite passes.

Technical Event Head — Circuit Fixer **Oct 2026**

MindSpark '26, COEP Technological University *Pune, Maharashtra*

- Engineered multi-stage hardware troubleshooting challenges (op-amp stability, digital IC race conditions, and parasitic faults) evaluating circuit debugging skills of **200+ collegiate participants**.

Remote VLSI Intern **Apr 2026 – July 2026**

LaunchEd Global *Remote*

- Completed guided training in ASIC design flow: RTL Verilog modeling, functional simulation, and basic static timing checks.

Hardware & RF Engineering Projects

CSAT-2 Dual-Band Satellite RF Switching Board | *KiCad 4-Layer, CPWG Routing* | 3D Model **Sep 2026 – Oct 2026**

- Redesigned satellite RF switching board from 200×100 mm to 75×75 mm (**71.8% area reduction**) with custom CubeSat rail cutouts (autode.sk/4dCDkl9).
- Integrated TI CC1120 sub-GHz transceiver and Qorvo QPA9510SR PA; routed 50 Ω coplanar waveguides with ground (CPWG) and via-stitching fences for cross-talk isolation; board prepared for laboratory fabrication.
- Separately tuned UHF (435 MHz) antenna matching assembly on calibrated Vector Network Analyzer (VNA), achieving **1.009:1 VSWR (47.0 dB Return Loss)**.

Cognitive Electronic Warfare Spectrum Sensing via POMDP | *DRDO Defense Submission* **Sep 2026 – Oct 2026**

- Formulated dynamic spectrum monitoring under instantaneous receiver bandwidth limits as a 7-tuple Partially Observable Markov Decision Process (**POMDP**) for the Smart India Hackathon DRDO problem statement.
- Derived Bayesian belief-state update models balancing wideband sweeping against narrowband dwell for blind signal detection.

Electrode Lead Driver & Biopotential Analog Front-End | *Analog Design, SPICE, Differential MOSFET* **Aug 2026 – Sep 2026**

- Designed a high-gain, low-noise analog differential electrode driver stage achieving > 80 dB CMRR to reject 50 Hz environmental power-line interference in SPICE simulations.

Transistor-Level Custom Complementary Logic Modeling | *SPICE, Transistor Primitives, Custom Cell* **May 2026 – July 2026**

- Modeled custom logic cell primitives directly at the transistor level using complementary MOSFET networks without HDL abstraction; analyzed propagation delay and dynamic switching characteristics in SPICE.

Technical Skills & Affiliations

EDA & Simulation Tools: KiCad (4-Layer RF Layout), SPICE, MATLAB, Autodesk Fusion 360
RF & Lab Instrumentation: Vector Network Analyzers (VNA), Digital Storage Oscilloscopes, Signal Generators, S-Parameters, Smith Charts
Hardware Concepts: Coplanar Waveguides (CPWG), Impedance Matching, VSWR Tuning, Link Budgets, Transistor-Level Circuit Design
Languages & Firmware: C (ISO C99), Python, Embedded C, Bash, Git
Professional Affiliations & Service: Student Member & Volunteer, **IEEE** (IEEE Pune Section; active attendee and student volunteer across conferences and Student Congresses)