Design, Validation, Testing and Fabrication of a Reconfigurable Reverse-Logic Combinational Circuit

A Physical Building Block for Boolean Satisfiability

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September 13, 2026

Document Type:	Product Requirements Document (PRD)
Project Stage:	Concept Definition and Architecture
Target Prototype:	Four-variable reverse-logic expression block
Primary Primitives:	Reverse AND and Reverse OR

Executive objective. This project investigates whether Boolean constraints can be physically propagated in the reverse direction using fabricated logic primitives. The first prototype is a reconfigurable four-variable expression block containing one reverse AND gate and multiple reverse OR gates. Multiple blocks are intended to form a larger PCB-level constraint network for experimental investigation of Boolean satisfiability.

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1 Document Purpose

This Product Requirements Document defines the functional, architectural, electrical, verification, fabrication and testing requirements for a reconfigurable reverse-logic combinational circuit.

The immediate objective is to design and fabricate a physical building block capable of performing reverse Boolean operations for AND and OR functions.

The longer-term objective is to compose multiple such blocks into a physical constraint network for Boolean Satisfiability (SAT).

The document deliberately separates:

1. the mathematical definition of reverse logic;
2. the first fabricated chip;
3. the PCB-level search architecture; and
4. the eventual SAT interpretation.

This separation prevents the first fabrication from being treated as a complete SAT solver. The first fabrication establishes the physical validity and composability of the underlying reverse-logic primitive.

2 Executive Summary

A conventional Boolean gate evaluates a function in the forward direction:

$$Y = f(A, B). \tag{1}$$

The proposed reverse gate operates from a specified output value Y and produces a valid pair of inputs (A, B) satisfying:

$$f(A, B) = Y. \tag{2}$$

For functions with multiple valid input combinations, the reverse gate selects one valid combination. Repeated evaluations shall permit exploration of alternative valid assignments.

The first chip shall contain one reverse AND gate and multiple reverse OR gates. Select lines shall configure the expression implemented by the chip for a four-variable problem.

The output states shall use a three-level electrical encoding:

$$+5\,\mathrm{V} \equiv 1, \qquad -5\,\mathrm{V} \equiv 0, \qquad 0\,\mathrm{V} \equiv \text{INVALID}. \tag{3}$$

At the PCB level, multiple chips may be interconnected through conventional logic, other reverse-logic blocks and feedback paths. The resulting system shall be studied as a physical mechanism for candidate generation, constraint propagation and candidate rejection.

A successful SAT result requires discovery of a globally satisfying assignment. An UNSAT result requires exhaustive or otherwise formally justified elimination of the relevant search space; random sampling alone shall not constitute an UNSAT proof.

3 Research Question

The primary research question is:

Can physically implemented inverse Boolean relations be composed into a practical hardware architecture for constraint propagation and experimental Boolean satisfiability search?

The first phase addresses the narrower question:

$$\boxed{\begin{array}{l}\text{Can AND and OR Boolean constraints be implemented}\\ \text{as reliable two-output reverse-logic primitives in silicon?}\end{array}} \tag{4}$$

Subsequent phases shall investigate whether such primitives provide useful system-level properties when composed through multiple chips and feedback.

4 Scope

4.1 In Scope

The first project phase includes:

- mathematical definition of reverse AND and reverse OR;
- truth-table and assignment-space verification;
- four-variable expression architecture;
- one reverse AND primitive;
- multiple reverse OR primitives;
- configurable expression selection;
- three-state electrical output representation;
- repeated evaluation of multi-solution reverse mappings;
- transistor-level circuit design;
- SPICE verification;
- physical layout;
- DRC and LVS;
- post-layout verification;
- fabrication;
- laboratory characterization;
- multi-chip composability testing.

4.2 Out of Scope for the First Fabrication

The following are not required to be solved in the first fabricated chip:

- an unrestricted general-purpose SAT solver;
- arbitrary numbers of Boolean variables;
- arbitrary Boolean gate types;
- a proof of computational advantage over software SAT solvers;
- a guaranteed polynomial-time SAT algorithm;
- a complete UNSAT proof mechanism implemented entirely within the first chip;
- large-scale PCB integration.

These are future research questions rather than first-prototype acceptance criteria.

5 System Architecture

The project is divided into three abstraction levels.

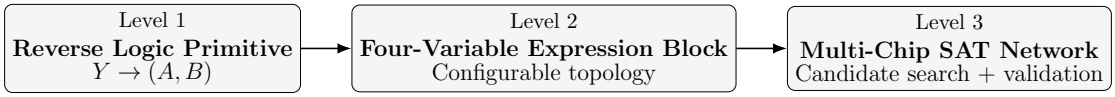


Figure 1: Three abstraction levels of the proposed research system.

5.1 Level 1: Reverse Logic Primitive

Every reverse gate shall have exactly one logical input Y and two logical outputs A and B.

For a forward Boolean function

$$Y = f(A, B), \tag{5}$$

the reverse operation is represented as

$$R_f(Y) \rightarrow (A, B) \tag{6}$$

with the validity condition

$$f(A, B) = Y. \tag{7}$$

Only reverse AND and reverse OR are included in the first prototype.

5.2 Level 2: Four-Variable Expression Block

The first chip shall contain:

- one reverse AND gate;

- multiple reverse OR gates;
- configurable interconnection paths;
- select lines;
- one enable input;
- one target-value input Y;
- assignment outputs.

The expression block shall operate on four Boolean variables

$$X_1, X_2, X_3, X_4. \tag{8}$$

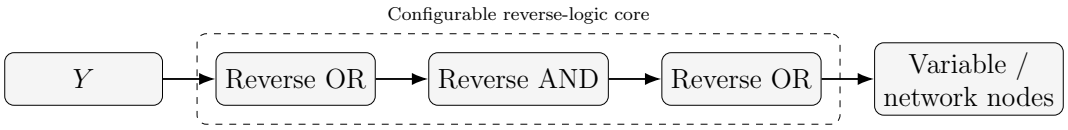


Figure 2: Illustrative four-variable expression-block topology. The exact interconnection and select-line encoding shall be frozen during architecture definition.

The exact number of output and select pins shall be frozen during architecture definition after the expression configuration set is specified.

5.3 Level 3: Multi-Chip SAT Network

Multiple expression blocks shall be interconnected externally on a PCB.

The intended architecture is:

The final PCB architecture shall be specified only after the single-chip primitive has been experimentally validated.

6 Mathematical Definition

Let

$$f : \{0,1\}^2 \to \{0,1\} \tag{9}$$

be a Boolean function.

For a specified output $y \in \{0,1\}$, define the satisfying preimage set:

$$S_y(f) = \left\{(A,B) \in \{0,1\}^2 \mid f(A,B) = y\right\}. \tag{10}$$

The reverse gate shall produce

$$(A,B) \in S_y(f). \tag{11}$$

Therefore, the reverse operation is a relation rather than necessarily a unique inverse function.

If

$$|S_y(f)| = 1, \tag{12}$$

the output assignment is unique.

If

$$|S_y(f)| > 1, \tag{13}$$

the implementation must select one of multiple valid assignments.

This distinction is central to the proposed architecture.

7 Reverse AND

The forward AND function is

$$Y = A \wedge B. \tag{14}$$

The reverse AND relation is:

$$R_{\text{AND}}(Y) \to (A, B) \tag{15}$$

subject to

$$A \wedge B = Y. \tag{16}$$

Table 1: Complete reverse AND assignment mapping.

Y	Valid assignments (A, B)	Number of assignments
0	$(0,0), (0,1), (1,0)$	3
1	$(1,1)$	1

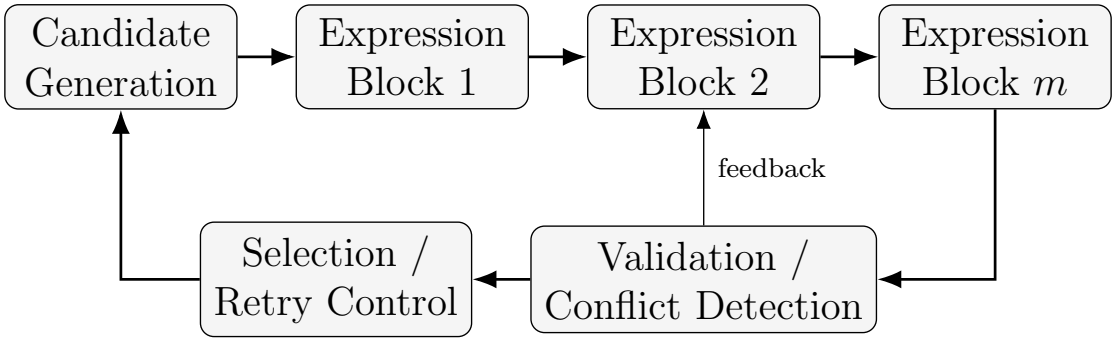


Figure 3: Conceptual PCB-level architecture. Feedback and control are system-level functions; the individual reverse gate remains combinational.

For $Y = 1$, the assignment is deterministic:

$$Y = 1 \Rightarrow (A, B) = (1, 1). \tag{17}$$

For $Y = 0$, three assignments satisfy the relation:

$$Y = 0 \Rightarrow (A, B) \in \{(0, 0), (0, 1), (1, 0)\}. \tag{18}$$

The assignment-selection mechanism shall therefore support repeated evaluation for this case.

8 Reverse OR

The forward OR function is

$$Y = A \vee B. \tag{19}$$

The reverse OR relation is:

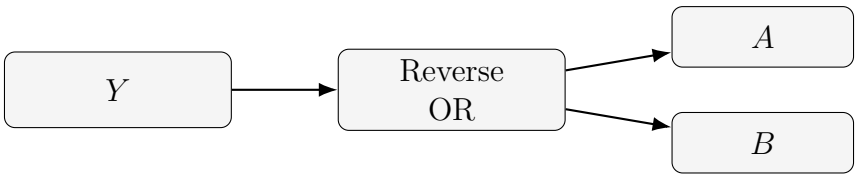
$$R_{\mathrm{OR}}(Y) \rightarrow (A, B) \tag{20}$$

subject to

$$A \vee B = Y. \tag{21}$$

Table 2: Complete reverse OR assignment mapping.

Y	Valid assignments (A, B)	Number of assignments
0	$(0, 0)$	1
1	$(0, 1), (1, 0), (1, 1)$	3



Constraint:
$A \vee B = Y$

Figure 4: Functional representation of the reverse OR primitive.

For $Y = 0$:

$$Y = 0 \Rightarrow (A, B) = (0, 0). \tag{22}$$

For $Y = 1$:

$$Y = 1 \Rightarrow (A, B) \in \{(0, 1), (1, 0), (1, 1)\}. \tag{23}$$

9 Reverse Evaluation and Assignment Selection

A reverse gate with multiple valid assignments must select one assignment during an evaluation.

The general model is:

$$R_f(Y, q) \rightarrow (A, B), \tag{24}$$

where q denotes the assignment-selection state.

The required correctness condition is:

$$f(A, B) = Y. \tag{25}$$

The first prototype shall investigate an assignment-selection mechanism capable of producing different valid assignments across repeated evaluations.

Candidate mechanisms include:

1. externally supplied pseudo-random selection;
2. deterministic cycling through valid assignments;
3. internally generated pseudo-random state;
4. analog-noise-assisted selection;
5. a hybrid approach.

The final selection mechanism shall be frozen during the detailed architecture phase after electrical feasibility, repeatability and fabrication constraints are evaluated.

9.1 Important Architectural Boundary

The fabricated reverse gate shall remain a combinational relationship at the logical level.

Repeated evaluation, randomness, retry control and feedback shall be treated as system-level mechanisms unless a future revision explicitly introduces state into the chip.

This distinction permits:

$$\boxed{\text{combinational reverse primitive} + \text{external evaluation control}} \tag{26}$$

without defining the individual gate as a sequential state machine.

10 Configuration Model

For k binary select lines, the configuration space contains:

$$N_{\text{config}} = 2^k \tag{27}$$

possible code words.

The final architecture shall classify every code word as either:

1. supported configuration;
2. reserved configuration with defined behavior.

No configuration shall be left with unspecified electrical or logical behavior.

The configuration table shall contain, at minimum:

Table 3: Required configuration-table structure.

SEL	Expression ID	Boolean expression	Status
$000\ldots0$	E0	$F_0(X_1, X_2, X_3, X_4)$	Supported
$000\ldots1$	E1	$F_1(X_1, X_2, X_3, X_4)$	Supported
$\vdots$	$\vdots$	$\vdots$	$\vdots$
$111\ldots1$	E_{N-1}	Defined behavior	Supported/Reserved

11 Signal and Electrical Interface

The proposed chip-level electrical interface is:

Signal	**Type**	**Function**
V_{CC}	Supply	Positive supply, nominally $+5\,\mathrm{V}$.
V_{DD}	Supply	Negative supply, nominally $-5\,\mathrm{V}$.
GND	Reference	$0\,\mathrm{V}$ electrical reference.

Y	Input	Target Boolean value presented to the reverse expression block.
SEL	Input	Configuration code selecting the supported four-variable expression.
EN	Input	Enables or disables the expression block according to the final interface specification.
O_i	Output	Physical Boolean assignment or intermediate reverse-logic node, according to the final pinout.

The exact number of assignment-output pins shall be determined after the four-variable expression topology is frozen.

11.1 Electrical State Encoding

The proposed logical encoding is:

$$+5\,\mathrm{V} \equiv 1 \tag{28}$$

$$-5\,\mathrm{V} \equiv 0 \tag{29}$$

$$0\,\mathrm{V} \equiv \text{INVALID}. \tag{30}$$

The actual input and output acceptance thresholds shall not be assumed to be exactly $+5\,\mathrm{V}$, $-5\,\mathrm{V}$ and $0\,\mathrm{V}$ in the transistor implementation. Threshold windows shall be established from the selected fabrication process, circuit topology and noise margins.

12 Invalid State and Conflict Detection

The $0\,\mathrm{V}$ state is reserved as an explicit invalid or conflict state.

For a set of candidate outputs

$$O_1, O_2, \ldots, O_n, \tag{31}$$

define the state-validity indicator:

$$C_i = \begin{cases} 1, & O_i \text{ is a valid Boolean state} \\ 0, & O_i \text{ is INVALID.} \end{cases} \tag{32}$$

A candidate is accepted only if:

$$C_{\text{candidate}} = \bigwedge_{i=1}^{n} C_i = 1. \tag{33}$$

Therefore,

$$\exists i : \ O_i = \text{INVALID} \Rightarrow C_{\text{candidate}} = 0. \tag{34}$$

This definition concerns physical validity of the generated candidate. It is distinct from the mathematical statement that the complete Boolean instance is UNSAT.

13 Constraint Propagation

Let a Boolean instance contain expressions:

$$F_1(X_1, \ldots, X_n), F_2(X_1, \ldots, X_n), \ldots, F_m(X_1, \ldots, X_n). \tag{35}$$

The SAT condition is:

$$F(X_1, \ldots, X_n) = \bigwedge_{j=1}^{m} F_j(X_1, \ldots, X_n) = 1. \tag{36}$$

A reverse expression block attempts to generate assignments consistent with its specified target value.

When multiple blocks are interconnected, a candidate assignment must satisfy all applicable constraints simultaneously.

The system therefore follows the conceptual process:

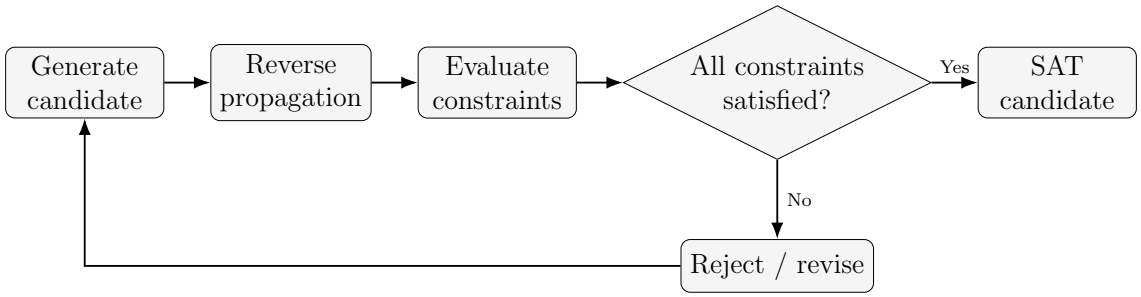


Figure 5: Conceptual candidate-evaluation cycle for the PCB-level system.

14 SAT and UNSAT Semantics

The project shall explicitly distinguish three outcomes.

14.1 SAT

A Boolean instance is experimentally classified as SAT when the physical system produces a candidate assignment

$$X^* = (x_1^*, \ldots, x_n^*) \tag{37}$$

for which:

$$F_j(X^*) = 1 \qquad \forall j \in \{1, \ldots, m\}. \tag{38}$$

The assignment shall be independently verified using a trusted digital reference model.

14.2 Candidate Failure

If a generated candidate produces an invalid state or violates one or more constraints, the result is:

$$\text{candidate rejected.} \tag{39}$$

This does not imply:

$$\text{UNSAT.} \tag{40}$$

14.3 UNSAT

A mathematically valid UNSAT result requires elimination of every assignment in the defined search space or another formally justified proof of unsatisfiability.

Random sampling alone shall not be accepted as an UNSAT proof.

This requirement is essential to the scientific interpretation of the proposed architecture.

15 Feedback Architecture

Feedback is a system-level research mechanism.

A candidate generated by one or more reverse blocks may be evaluated by downstream constraints. The resulting validation information may influence a subsequent candidate-generation cycle.

The conceptual loop is:

$$\boxed{\begin{array}{c}\text{Candidate} \rightarrow \text{Constraint Evaluation} \rightarrow \text{Conflict Information} \\ \rightarrow \text{Candidate Revision} \rightarrow \text{Candidate}\end{array}} \tag{41}$$

The first fabricated chip shall not require stateful feedback inside the reverse primitive.

Feedback shall initially be implemented and evaluated at the PCB level.

16 Functional Requirements

ID	Requirement
FR-001	The first fabrication shall implement reverse AND and reverse OR only.
FR-002	Every reverse primitive shall have exactly one logical input and two logical outputs.
FR-003	The reverse AND primitive shall satisfy $A \wedge B = Y$ for every valid evaluation.
FR-004	The reverse OR primitive shall satisfy $A \vee B = Y$ for every valid evaluation.
FR-005	The first chip shall contain one reverse AND gate.
FR-006	The first chip shall contain multiple reverse OR gates.
FR-007	The first chip shall support configurable four-variable Boolean expressions.
FR-008	Select lines shall determine the supported expression configuration.
FR-009	Every supported select-line configuration shall have a defined Boolean expression.
FR-010	The chip shall provide an enable input.
FR-011	The proposed electrical representation shall distinguish +5 V, −5 V and 0 V states.
FR-012	0 V shall represent an invalid/conflict state at the logical interface.
FR-013	Repeated evaluations shall permit exploration of multiple valid assignments where the reverse relation has multiple solutions.
FR-014	The reverse primitive shall remain combinational at the logical level in the first fabrication.
FR-015	The chip interface shall support cascading and external interconnection subject to electrical fan-out and loading limits.
FR-016	The PCB-level architecture shall permit feedback and retry mechanisms.
FR-017	Generated candidates shall be independently checked against a digital reference model during validation.

17 Non-Functional Requirements

ID	Requirement
NFR-001	The circuit shall operate within the voltage, current and temperature limits of the selected fabrication process.
NFR-002	The implementation shall provide adequate noise margins for the three-state electrical representation.
NFR-003	The output shall meet defined loading and fan-out requirements.
NFR-004	The circuit shall be testable through accessible electrical nodes or dedicated test structures where required.
NFR-005	The layout shall satisfy the fabrication process design rules.

NFR-006	The final layout shall pass DRC and LVS before fabrication.
NFR-007	Post-layout simulation shall be performed with extracted parasitics.
NFR-008	The design shall maintain traceability between mathematical specification, circuit implementation and measured silicon behavior.

18 Verification Strategy

Verification shall proceed from the highest abstraction level toward the fabricated device.

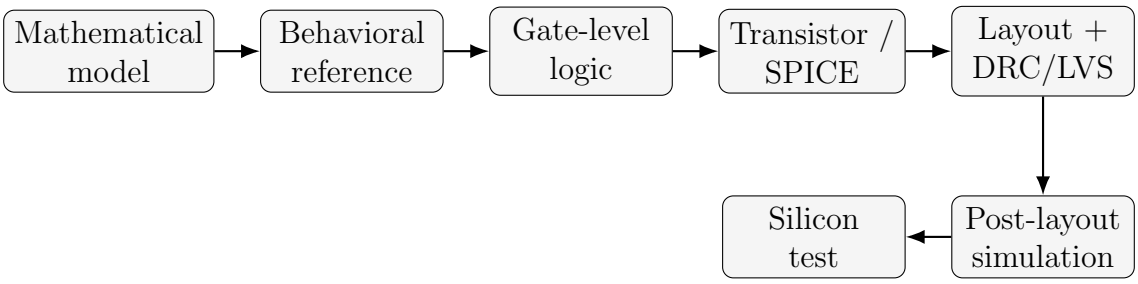


Figure 6: Verification and implementation flow.

19 Mathematical Verification

For each reverse primitive, all four possible (A, B) combinations shall be enumerated.

For AND:

$$\{00, 01, 10, 11\} \tag{42}$$

shall be checked against the forward function.

For OR, the same complete input space shall be checked.

For each target Y, the reference implementation shall generate the complete set $S_Y(f)$.

Hardware-generated assignments shall satisfy:

$$(A, B) \in S_Y(f). \tag{43}$$

The reference model shall therefore act as the oracle for functional verification.

20 Circuit-Level Verification

The transistor-level implementation shall be verified for:

- correct DC operating points;
- valid 1 and 0 output levels;
- valid invalid-state generation where applicable;

- propagation delay;
- output drive;
- input and output loading;
- power consumption;
- supply sensitivity;
- process corners;
- temperature corners;
- Monte Carlo variation;
- startup and transition behavior.

The final limits shall be defined using the selected process design kit and the intended external interface.

21 Physical Design and Fabrication

The physical implementation shall follow the selected process design kit.

The layout shall account for:

- positive and negative supply distribution;
- ground distribution;
- substrate and well connections;
- input protection as required;
- output drivers;
- signal isolation;
- test access;
- power integrity;
- parasitic effects.

The final layout shall satisfy:

$$\mathrm{DRC} = 0 \tag{44}$$

and

$$\mathrm{LVS} = 0. \tag{45}$$

Parasitic extraction shall be followed by post-layout simulation.

22 Silicon Testing

Fabricated devices shall undergo laboratory characterization.

The test sequence shall include:

1. supply verification;
2. ground and reference verification;
3. input-state verification;

4. enable verification;
5. configuration verification;
6. reverse AND functional testing;
7. reverse OR functional testing;
8. repeated-evaluation testing;
9. assignment-diversity testing;
10. output-voltage characterization;
11. loading and fan-out testing;
12. propagation-delay measurement;
13. power measurement;
14. process/sample variation analysis where sufficient samples are available.

23 Assignment-Diversity Experiment

For reverse OR with $Y = 1$, the valid assignment set is:

$$S_1(\mathrm{OR}) = \{(0,1),(1,0),(1,1)\}. \tag{46}$$

For reverse AND with $Y = 0$:

$$S_0(\mathrm{AND}) = \{(0,0),(0,1),(1,0)\}. \tag{47}$$

Repeated evaluations shall determine whether the implementation explores more than one valid assignment.

For a chosen selection mechanism, the measured frequency

$$\hat{p}_i = \frac{N_i}{N} \tag{48}$$

shall be recorded for each assignment i, where N_i is the number of observed occurrences and N is the total number of evaluations.

The observed distribution shall be compared with the intended selection model.

No assumption of uniformity shall be made unless uniform random selection is explicitly chosen as the design objective.

24 Testing the Four-Variable Block

The four-variable block shall be tested at three levels.

24.1 Configuration Test

Every supported select-line combination shall be applied and verified against its documented expression.

24.2 Functional Test

For each supported expression, relevant target values and generated assignments shall be checked against the reference model.

24.3 Composability Test

The output of one reverse block shall be connected to the input interface of another compatible block or test circuit.

The following shall be measured:

- voltage integrity;
- loading;
- fan-out;
- timing;
- functional correctness.

25 Research and Development Flow

The project shall follow the staged development process shown in Figure 7.

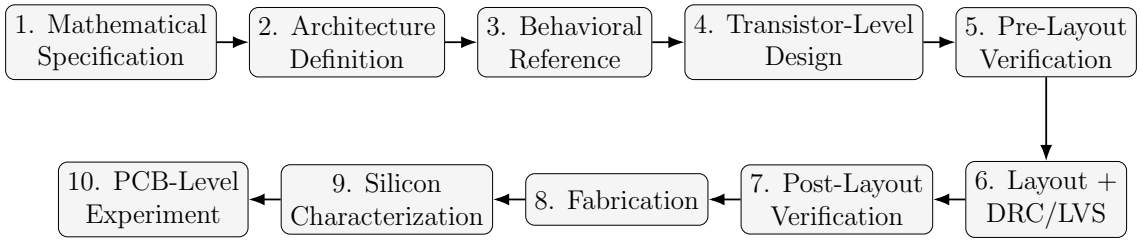


Figure 7: Proposed research and development flow.

Progression to each stage shall depend on successful verification of the preceding stage.

26 Deliverables

The project shall produce the following artefacts:

1. Product Requirements Document.
2. Formal mathematical definition of reverse AND and OR.
3. Complete reverse truth tables.
4. Four-variable expression architecture.
5. Configuration encoding and truth table.
6. Behavioral reference model.
7. Gate-level design.
8. Transistor-level schematics.
9. SPICE simulation environment.

10. Pre-layout verification results.
11. Physical layout.
12. DRC-clean layout.
13. LVS-clean layout.
14. Post-layout simulation results.
15. Fabrication database.
16. Silicon test plan.
17. Silicon measurement data.
18. Comparison of mathematical, simulated and measured behavior.
19. PCB-level interconnection specification.
20. Experimental evaluation of repeated reverse evaluations.

27 Acceptance Criteria

The first fabricated prototype shall satisfy the following criteria.

ID	Acceptance Criterion	Evidence
AC-001	Reverse AND produces only assignments satisfying $A \wedge B = Y$.	Measured truth table.
AC-002	Reverse OR produces only assignments satisfying $A \vee B = Y$.	Measured truth table.
AC-003	Every supported configuration produces the documented expression.	Configuration test data.
AC-004	Multiple valid assignments are experimentally observable where the mathematical relation contains multiple solutions.	Repeated-evaluation dataset.
AC-005	The electrical interface distinguishes the three defined states within the specified thresholds.	Voltage characterization.
AC-006	The fabricated circuit operates within the specified electrical and environmental limits.	Characterization report.
AC-007	The layout passes DRC and LVS before fabrication.	EDA verification reports.
AC-008	Post-layout simulation agrees with the functional requirements.	Simulation report.
AC-009	The chip supports the defined external loading and interconnection conditions.	Composability test.
AC-010	At least one supported four-variable expression is demonstrated end-to-end against the reference model.	Experimental demonstration and reference-model comparison.

28 Risks and Research Questions

The following items shall remain explicit research questions rather than hidden assumptions.

Area	Risk / Question	Mitigation / Study
Electrical	The +5 V, 0 V and −5 V states may require careful threshold and noise-margin design.	Define threshold windows using the selected process and perform corner/Monte Carlo analysis.
Assignment selection	A reverse relation may have multiple valid assignments.	Evaluate deterministic and stochastic selection mechanisms before architecture freeze.
Global consistency	A locally valid assignment may violate another constraint.	Use explicit validation and feedback at the PCB level.
UNSAT detection	Random trials do not prove UNSAT.	Separate candidate discovery from exhaustive/formal UNSAT determination.
Interconnection	Reverse outputs may experience loading or fan-out limitations.	Characterize drivers, receivers and maximum fan-out.
Scalability	A small expression block may not scale efficiently to larger SAT instances.	Measure resource growth experimentally before claiming scalability.
Fabrication	Process variation may affect multi-level voltage discrimination.	Use process corners, Monte Carlo analysis and silicon characterization.

29 Expected Research Outcome

The immediate expected outcome is a validated physical implementation of reverse AND and reverse OR relations.

The second outcome is a configurable four-variable reverse-logic expression block suitable for interconnection with additional blocks.

The broader research outcome is an experimental assessment of whether reverse Boolean constraint propagation, repeated assignment generation and feedback provide a useful architecture for physical SAT computation.

The project does not assume in advance that the proposed architecture will outperform conventional digital or software SAT solvers.

Instead, the project shall establish experimentally:

$$\boxed{\begin{array}{l}\text{What the architecture can compute and how reliably it computes it,}\\ \text{and under what constraints it remains practical.}\end{array}} \tag{49}$$

30 Future Extensions

Subject to successful completion of the first prototype, future work may investigate:

- additional reverse Boolean primitives;
- larger variable counts;
- larger expression counts;
- automated configuration generation;
- deterministic exhaustive search;
- pseudo-random candidate search;
- adaptive candidate selection;
- hardware conflict propagation;
- feedback-based search;
- parallel candidate evaluation;
- FPGA or ASIC-level system integration;
- comparison with conventional SAT architectures.

These extensions shall not alter the acceptance criteria of the first fabricated reverse-logic block.

31 Conclusion

This project proposes a staged investigation into the physical implementation of inverse Boolean relations.

The fundamental operation is:

$$\boxed{Y = f(A, B) \quad \Longrightarrow \quad Y \to (A, B)} \tag{50}$$

with the generated assignment required to satisfy the original Boolean relation.

The first fabricated device shall implement one reverse AND gate and multiple reverse OR gates within a configurable four-variable expression block.

Repeated evaluations shall investigate the exploration of multiple valid assignments. Multiple chips shall subsequently be combined at PCB level to study constraint propagation, feedback and physical SAT search.

The project therefore proceeds from a well-defined mathematical primitive to a measurable silicon implementation and only then to a larger computational architecture.