Lakshya Varshney

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LinkedIn GitHub Portfolio Credly

Education

COEP Technological University **Pune, Maharashtra**

B.Tech. in Electronics and Telecommunication Engineering (CGPA: 8.16/10) *Expected July 2029*

- **Relevant Coursework:** Formal Verification, RF & Microwave Engineering, Analog IC Design, VLSI Design, Embedded Systems, Signal Processing, Compilers & Systems Programming, Data Structures.

Professional Experience & Technical Leadership

RF & Communications Subsystem Contributor **Nov 2025 – Present**

COEP Satellite Initiative (CSAT-2) *Pune, Maharashtra*

- Engineered **NEST**, an enterprise system of record migrating satellite asset tracking from spreadsheets to an auditable PostgreSQL/NestJS/React platform.
- Designed and routed a 4-layer RF transceiver and switching board in KiCad tailored to CubeSat 1U structural rail cutouts.
- Conducted laboratory VNA testing, RF impedance matching, and link budget calculations for ground station operations.

Technical Event Head — Circuit Fixer **Oct 2026**

MindSpark '26, COEP Technological University *Pune, Maharashtra*

- Spearheaded technical problem design and bench evaluation for COEP's premier hardware debugging competition, evaluating op-amp stability, digital race conditions, and circuit diagnosis for **200+ collegiate participants**.

Remote VLSI Intern **Apr 2026 – July 2026**

LaunchEd Global *Remote*

- Completed guided curriculum in ASIC design flow: RTL Verilog programming, functional simulation, and basic static timing checks.

Systems Software & EDA Projects

LogiSAT: Automated Circuit Equivalence & Fault Verifier (ATPG) | *ISO C99, DPLL, GTest* **Oct 2026**

- Built an open-source formal verification tool from scratch in strict ISO C99 with zero dynamic heap allocation on search trail stacks (GitHub | DOI: 10.5281/zenodo.24085901).
- Implemented linear-size Tseytin transformation to 3-CNF, Miter circuit construction for Combinational Equivalence Checking (CEC), and Automatic Test Pattern Generation (ATPG) for single stuck-at faults (s-a-0 / s-a-1).
- Automated regression tests via Google Test (**12/12 unit tests passing, Valgrind certified zero leaks**) under `-Wall -Wextra -pedantic -std=c99`.

MISRA-C Embedded Scientific Calculator | *MISRA C:2012, Static Memory, Embedded C* **Sep 2026 – Oct 2026**

- Developed a scientific calculator in embedded C adhering strictly to core **MISRA C:2012** guidelines for safety systems (GitHub | DOI: 10.5281/zenodo.24085926).
- Enforced zero dynamic memory allocation (`malloc` prohibited), fixed-width standard integers (`stdint.h`), static buffer bounds checking, and defensive execution guarantees against undefined behavior.

Aakh: Automated Tech Feed & Model Pipeline | *Python, GitHub Actions CI/CD, REST API, React* **Aug 2026 – Present**

- Built an automated aggregator leveraging scheduled GitHub Actions workflows to scrape, summarize, and deploy technical feeds (GitHub | Live).
- Implemented dynamic model discovery protocol at runtime querying model provider REST endpoints, preventing failures from LLM deprecation.

Hardware, RF & Analog Engineering

CSAT-2 Dual-Band Satellite RF Switching Board | *KiCad 4-Layer, CPWG Routing* | 3D Model **Sep 2026 – Oct 2026**

- Redesigned satellite transceiver board from 200×100 mm to 75×75 mm (**71.8% area reduction**) with custom rail cutouts (autode.sk/4dCDkl9).
- Integrated TI CC1120 transceiver and Qorvo QPA9510SR PA; routed 50 Ω coplanar waveguides with ground (CPWG) and via-fences; board routing completed, awaiting fabrication.
- Separately performed lab VNA characterization of CSAT-2 UHF antenna matching assembly, achieving **1.009:1 VSWR (47.0 dB Return Loss)** at 435 MHz.

Electrode Lead Driver & Biopotential Analog Front-End | *Analog Design, SPICE, Differential MOSFET* **Aug 2026 – Sep 2026**

- Designed a high-gain, low-noise analog differential electrode driver stage achieving > 80 dB CMRR to reject 50 Hz environmental power-line interference with sub-microamp patient leakage safety in SPICE simulations.

Transistor-Level Custom Complementary Logic Modeling | *SPICE, Transistor Primitives, Custom Cell* **May 2026 – July 2026**

- Designed custom logic cell primitives directly at the transistor level using complementary MOSFET networks without HDL abstraction; evaluated propagation delay tradeoffs in SPICE.

Research & Technical Specifications

Reverse-Logic ASIC Building Block PRD | *Silicon Architecture, Hardware SAT* **Sep 2026**

- Authored Product Requirements Document and circuit architecture for a fabricated 4-variable reconfigurable reverse-logic expression block evaluating physical Boolean constraint propagation.
- Specified reverse AND/OR primitives for PCB constraint networks, targeting hardware-accelerated Boolean satisfiability solving.
- Characterized bidirectional propagation dynamics, signal pinout constraints, and board-level test methodologies for silicon validation.

Cognitive Electronic Warfare Spectrum Sensing via POMDP | *DRDO Defense Submission* **Sep 2026 – Oct 2026**

- Formulated dynamic electronic surveillance under receiver bandwidth limits as a 7-tuple Partially Observable Markov Decision Process (**POMDP**) for the Smart India Hackathon DRDO problem statement.
- Derived Bayesian belief-state updates balancing wideband exploration vs. narrowband dwell to classify modulations under negative SNR.

Academic Honors, Community & Social Impact

Indian Olympiad Qualifier in Mathematics (IOQM) **National Examination**

National Mathematics Olympiad Pedigree *Conducted by MTA / HBCSE*

- Qualified national-tier mathematics competition evaluating advanced combinatorial analysis, number theory, and geometry.

IEEE Student Member & Conference Volunteer **2025 – Present**

IEEE Pune Section *Pune, Maharashtra*

- Active student volunteer and attendee across regional conferences and Student Congresses, assisting with event organization and logistics.

2nd Place — Forbes Marshall Engineering Ideathon **Pune, Maharashtra**

Technical Case Competition *MindSpark / Industry Review*

- Awarded 2nd place in engineering design thinking, constraint optimization, and industrial product architecture.

Student Volunteer **May 2026 – June 2026**

A Ray Of Hope Charitable Trust *Pune, Maharashtra*

- Participated in community social internship organizing educational material distribution, tree plantations, and local welfare activities.

Technical Skills & Affiliations

Languages & Standards: ISO C99, Lean 4, C++, MISRA C:2012, Python, TypeScript, SQL, Bash, Verilog (Basics)
EDA & Systems Concepts: Formal Equivalence Checking (CEC via Miter), SAT Solvers (DPLL Algorithm), Tseytin Transformation, ATPG (Stuck-At Faults), Static Timing Analysis, Combinational Logic Synthesis, Static Memory Analysis
RF & Hardware Tools: KiCad (4-Layer RF Layout), SPICE, MATLAB, VNA, Digital Storage Oscilloscopes, Signal Generators, CPWG, S-Parameters, VSWR Tuning
Tools & Frameworks: Google Test (GTest), Valgrind, GCC / Clang / MinGW, GNU Make, Lake, Git, PostgreSQL, NestJS, React, LaTeX
Professional Affiliations & Service: Student Member & Volunteer, **IEEE** (IEEE Pune Section; active attendee and student volunteer across conferences and Congresses)
Literary Works: Author, *Ink & Infinity*; Featured Verse, COEP Annual Literary Magazine (*The Truth That Walks Alone*)